configuration. The signals used by these LSIs are input, output, and processed using synchronizing clock signals. Generally, a device that operates on a synchronizing clock signal is structured so that the speed of its performance is proportional to the frequency of the clock signal. Typical devices operating on the synchronizing clock signal include CPUs (Central Processing Units), memories, and north bridges.

Also known today are devices acting on variable, not fixed operating frequencies. Many electronic devices such as personal computers, PDAs and cellular phones are designed to operate only as needed. In more and more systems, their operating frequency is lowered in standby mode or in sleep mode in order to attain a reduced level of power dissipation; when a call is being made or moving picture signals are being processed, the operating frequency is raised to accelerate the processing of the systems. (One such system is disclosed illustratively in Japanese Patent Laid-open No. 2000-163965.)

These systems with their operating frequencies made variable usually have their functional parts divided in two regions. One region for which the operating frequency must remain fixed is isolated from the other region fed with a clock signal at variable frequencies. This

structure is intended to prevent the region of the parts operating at variable frequencies from adversely affecting the other region of fixed-frequency parts.

Meanwhile, the information processing apparatuses using a synchronizing signal at varied frequencies are required to provide steady performance regardless of their synchronizing signal being fixed or variable. Generally, if an apparatus is guaranteed to operate at a high frequency, i.e., at short clock intervals, the apparatus will also operate at reduced frequencies but the performance of its signal processing will be lowered in proportion to the drop in frequency. Although the dissipation of power is curtailed by simply reducing the operating speed in keeping with the lowered clock frequency, that is not an optimally controlled operating state. A more sophisticated control scheme has been called for.

The present invention has been made in view of the aforementioned technical problems and provides an information processing apparatus, an information storing apparatus, an information processing method, and an information processing program for implementing an optimal signal processing setup that ensures steady performance using variable operating frequencies.

Disclosure of Invention

In solving the foregoing and other technical problems and according to one aspect of the invention, there is provided an information processing apparatus including: a frequency information operating section for operating on frequency information about a synchronizing clock signal having a variable frequency; and an information processing section which is supplied with the synchronizing clock signal as an operating clock signal and which performs information processing in suitably timed relation with results of the operation by the frequency information operating section.

Where the information processing apparatus above of the invention is in use, the frequency information operating section of the apparatus admits frequency information about a synchronizing clock signal having a variable frequency and carries out such operations as adding up the frequency information or decoding the frequency information in encoded form. The information processing section of the apparatus performs information processing in accordance with the result of such operations. Having acquired the frequency information, the information processing section can proceed with its

processing in optimal fashion in a manner eliminating wasteful latency times.

According to another aspect of the invention, there is provided an information storing apparatus including: a frequency information operating section for operating on frequency information about a synchronizing clock signal having a variable frequency; and an information storing section which is supplied with the synchronizing clock signal as an operating clock signal and which performs an information storing operation in suitably timed relation with results of the operation by the frequency information operating section.

Where the information storing apparatus above of the invention is in use, the frequency information operating section of the apparatus similarly admits frequency information about a synchronizing clock signal having a variable frequency and carries out such operations as adding up the frequency information or decoding the frequency information in encoded form. The result of such operations is used by the inventive information storing apparatus as the basis for optimally storing information also in a manner eliminating wasteful latency times.

Brief Description of Drawings

Fig. 1 is a block diagram of an information processing apparatus embodying this invention.

Figs. 2A, 2B and 2C are timing charts in effect when a memory device is in operation, Fig. 2A showing how the device is timed to operate on a fixed-frequency clock signal, Fig. 2B depicting how the device operates in fixedly timed fashion on a variable clock frequency signal, Fig. 2C illustrating how the device operates in suitably timed relation with results from calculations of frequency information.

Figs. 3A and 3B are timing charts indicating examples of frequency information being used, Fig. 3A showing an example in which the frequency information denotes the frequency of a current operating clock signal CLKv, Fig. 3B depicting an example in which the frequency information is indexed to the frequency of the next clock interval preceding changes in the frequency of the operating clock signal CLKv.

Figs. 4A and 4B are tabular views showing examples of how frequency information is encoded, Fig. 4A showing an example in which the information is encoded in two bits, Fig. 4B illustrating an example in which the information is encoded using cyclically proportional

long as the operating clock signal is fixed at a predetermined frequency, optimization of the operations is relatively easy. That is, if an operation is made using the clock signal fixed at the frequency of 100 MHz as shown in Fig. 2A, the time parameters {Tras, Trcd, Trp} for this SDRAM are {40 ns, 20 ns, 20 ns}; if the CAS latency is 2, then the RAS activate time Tras is 4 clock intervals long, RAS-CAS delay time Trcd is 2 clock intervals long, and the precharge time Trp is 2 clock intervals long in latency. With these parameters in place, the operations are optimized at the fixed frequency of 100 MHz.

By contrast, when the operating clock signal is varied in frequency with the fixed-frequency control setup still in place, latency times occur in low frequency regions where each clock interval is prolonged. These latency times, when added up, can worsen the overall performance of the device. As shown in Fig. 2B, the first RAS activate time Tras with a leading edge at which the "A" command is issued remains four clock intervals long. Because the setup of Fig. 2B applies to a clock frequency of 50 MHz, half of the initial 100 MHz, the RAS activate time Tras is in fact 2 clock intervals longer than if the frequency of 100 MHz is in effect,

with the necessary wait time having already elapsed. The RAS activate time Tras for the next activate operation ("A") is 3 clock intervals longer than if the frequency of 100 MHz is in use. In like manner, the RAS-CAS delay time Trcd and the precharge time Trp involve prolonged latency times depending on the changes in the operating clock frequency.

The memory device of this embodiment performs its operation properly using the frequency information Infq when the operating clock signal is varied in frequency. As indicated in Fig. 2C, the signal processing is carried out in keeping with the frequency being used. The memory controller 12 is fed with the frequency information Infq from the frequency controlling section 13 as shown in Fig. 1. Given the frequency information Infq, the memory controller 12 calculates the clock signal period accordingly. If any command is found likely to be delayed when issued, the memory controller 12 causes the command in question to be issued earlier than usual for the memory 13 so that the latency time involved will be minimal. More specifically, as shown in Fig. 2C, the memory controller 12 receives from the frequency controlling section 13 the frequency information Infq saying that the clock frequency is 50 MHz after the

activate operation ("A") command is issued. The information is received at least one clock interval earlier than the time at which a read ("R") command is to be issued. Based on the received frequency information Infq, a clock pulse is first generated to give the timing for issuing the activate operation ("A") command, followed immediately by a clock pulse to give the timing for issuing the next read operation ("R") command. If the memory device of this embodiment were not used, the pulse to give the timing for issuing the read operation ("R") command would be 1 clock interval apart from the preceding interval as shown in Fig. 2A or 2B. With the memory device of this embodiment, by contrast, the memory controller 12 having received the frequency information Infq beforehand from the frequency controlling section 13 recognizes that the necessary operations are guaranteed even if pulses are generated consecutively to give the timing for issuing the activate operation ("A") command and the next read operation ("R") command. This allows the memory controller 12 optimally to control the memory 11 so that wasteful latency times are eliminated and overall performance is enhanced.

The memory controller can issue the read operation ("R") command on the condition that the RAS-CAS delay

time Trcd be met. The RAS-CAS delay time is a necessary wait time based on the frequency information Infq at least for the period from the time the issuance of the activate operation ("A") command has ended until the issuance of the next read operation ("R") command has ended. With the clock frequency assumed to be 100 MHz during issuance of the read operation ("R") command, the memory controller 12 can issue the read operation ("R") command on the condition that the RAS-CAS delay time Trcd as the required wait time be met, on the basis of the frequency information Infq in effect until the read operation ("R") command is issued.

Likewise, the memory controller based on the frequency information Infq issues the activate operation ("A") command and precharge operation ("P") command in such a manner that the necessary wait time is met and that the precharge time Trp and the RAS activate time Tras are optimally shortened.

What follows is a more detailed description of how the memory controller 12 recognizes beforehand that the necessary operations are guaranteed. In the setup of Fig. 2C, the second clock pulse is recognized to be 50 MHz and the clock interval is calculated at 20 ns based on the frequency information Infq. The RAS-CAS delay time Trcd

replaced by Article 34

S03P1219
REPLACED BY
ART 34 AMDT

CLAIMS

1. An information processing apparatus comprising:

a frequency information operating section for operating on frequency information about a synchronizing clock signal having a variable frequency; and

an information processing section which is supplied with said synchronizing clock signal as an operating clock signal and which performs information processing in suitably timed relation with results of the operation by said frequency information operating section.

2. The information processing apparatus according to claim 1, wherein said operation by said frequency information operating section on said frequency information about said synchronizing clock signal is intended to calculate a time for determining when to perform said information processing while said synchronizing clock signal is being supplied.

3. The information processing apparatus according to claim 1, wherein said frequency information about said synchronizing clock signal is constituted by either current or subsequent frequency information.

4. The information processing apparatus according to claim 1, wherein the operation on said frequency

information is carried out by decoding said frequency information in encoded form.

5. The information processing apparatus according to claim 1, wherein the operation on said frequency information is carried out by adding a corresponding signal cycle to the frequency in said frequency information.

6. An information storing apparatus comprising:

a frequency information operating section for operating on frequency information about a synchronizing clock signal having a variable frequency; and

an information storing section which is supplied with said synchronizing clock signal as an operating clock signal and which performs an information storing operation in suitably timed relation with results of the operation by said frequency information operating section.

7. The information storing apparatus according to claim 6, wherein said information storing section has a plurality of memory cells for storing data by accumulating electrical charges, and wherein said information storing operation includes at least one of the operations comprising bringing electrical charges from part of said memory cells to an amplifier, inputting and outputting electrical charges to and from said

amplifier, and causing said amplifier to accumulate electrical charges in said memory cells.

8. The information storing apparatus according to claim 7, wherein said memory cells are formed in a memory body, and wherein said frequency information operating section is formed in a memory control unit for controlling said memory body.

9. The information storing apparatus according to claim 6, wherein the operation on said frequency information is carried out by decoding said frequency information in encoded form.

10. The information storing apparatus according to claim 6, wherein the operation on said frequency information is carried out by adding a corresponding signal cycle to the frequency in said frequency information.

11. An information storing apparatus comprising:

a frequency controlling section for generating frequency information about a synchronizing clock signal having a variable frequency;

a frequency information operating section for operating on said frequency information; and

an information storing section which is supplied with said synchronizing clock signal as an operating

clock signal and which performs an information storing operation in suitably timed relation with results of the operation by said frequency information operating section.

12. The information storing apparatus according to claim 11, wherein said frequency controlling section varies said synchronizing clock signal in frequency based on a command coming from a central processing unit, in order to output frequency information about either the current or a subsequent frequency of said synchronizing clock signal.

13. An information processing method comprising the steps of:

operating on frequency information about a synchronizing clock signal having a variable frequency; and

supplying an information processing section with said synchronizing clock signal as an operating clock signal while allowing said information processing section to perform information processing in suitably timed relation with results of the operation in said frequency information operating step.

14. The information processing method according to claim 13, wherein said information processing includes storing information into a plurality of memory cells

capable of holding data through accumulation of electrical charges, said information processing further including at least one of the operations comprising bringing electrical charges from part of said memory cells to an amplifier, inputting and outputting electrical charges to and from said amplifier, and causing said amplifier to accumulate electrical charges in said memory cells.

15. An information processing program comprising the steps of:

operating on frequency information about a synchronizing clock signal having a variable frequency; and

supplying an information processing section with said synchronizing clock signal as an operating clock signal while allowing said information processing section to perform information processing in suitably timed relation with results of the operation in said frequency information operating step.

16. The information processing program according to claim 13, wherein said information processing includes storing information into a plurality of memory cells capable of holding data through accumulation of electrical charges, said information processing further

including at least one of the operations comprising bringing electrical charges from part of said memory cells to an amplifier, inputting and outputting electrical charges to and from said amplifier, and causing said amplifier to accumulate electrical charges in said memory cells.

THE FOLLOWING ARE THE ENGLISH TRANSLATION OF ANNEXES TO THE INTERNATIONAL PRELIMINARY EXAMINATION REPORT (ARTICLE 34):

Amended Sheets (Pages 2-6, 13-16, & 38-43/2)